

Description

Packet based telecommunications networks are being developed to carry Constant Bit Rate (CBR) data streams between a source and destination exchange in the form of multiplexed packets, or cells, which are recombined at the destination exchange into a CBR data stream. It is necessary in such a network to synchronise the frequency, and maintain the phase relation, of the recombined CBR stream with those of a source CBR stream arriving at the source exchange. The present invention relates to apparatus for, and a method of, achieving this synchronisation.

Figure 1 shows an Asynchronous Transfer Mode (ATM) transmission network for carrying CBR data streams in the form of ATM cells. A CBR data stream 2 arriving at a source exchange 4 is converted into ATM cells 6 which are transmitted across an ATM network 8 to a destination exchange 10. The ATM cells 6 are recombined at the destination exchange 10 into a CBR data stream 12. In carrying a CBR signal across a packet-based network the rate at which data leaves the destination exchange 10 should be the same as the rate at which it arrives at source exchange 4 requiring the frequency of the recombined CBR stream 12 and source CBR stream 2 to be synchronised.

One proposed method of frequency synchronisation is the use of residual time stamp (RTS) values which are calculated at the source exchange 4 using the frequency of the source CBR stream 2 and transmitted as part of the ATM cell 6 to the destination exchange 10 where the RTS values are used to calculate the frequency of the source CBR stream 2. Figure 1 shows such a system. A CBR line terminator 14 extracts the frequency 14A and data 14B associated with the CBR stream 2. The data 14B is diverted to a cell payload generator 16 which buffers and divides the data stream into data cells of the required number of bits. The data cells are converted into ATM cells 6 by ATM cell generator 18 which combines the data cells with a respective header generated by cell header generator 20. The header contains the RTS value generated by RTS generator 22 using the frequency 14A of the CBR stream 2.

At the destination exchange 10 the received ATM cells 6 are buffered in a cell buffer 38. The ATM cell header is processed by cell header processor 40 which extracts the received RTS value 42 whilst the ATM cell data is routed from the cell buffer 38 to a cell payload processor 43 before being recombined into a CBR stream 12 by CBR generator 48. The received RTS values 42 are used by calculating means 44 to calculate the source CBR frequency. The frequency of a local oscillator 46 is set to this calculated frequency which maintains the frequency of the recombined CBR stream 12.

RTS values are generated by the Synchronous Residual Time Stamp (SRTS) method which is standardised in International Consultative Committee for Telegraphs and Telephones (CCITT), now known as Interna-

tional Telecommunications Union (ITU), recommendation I-365, B-ISDN ATM adaption layer (AAL) specification, temporary document 60 SGXVIII, 1993 and described in US patent number 5,260,978. Figure 2 shows an RTS generator which uses the SRTS method. The method comprises continuously clocking a modulo sixteen counter 24 with a clock 26 which is related to a network reference frequency 28. Clock 26 is generated by dividing the network frequency reference 28 by an integer x using divider circuit 30. The value of x is defined in the CCITT recommendation and is a power of two which satisfies the condition

$$\text{twice CBR spot frequency} \geq \frac{\text{network frequency}}{x} \\ \geq \text{CBR spot frequency}$$

A counter reader 32 is arranged to sample the current value of the counter 24 every n cycles of source frequency, where n is defined by the CCITT recommendations. This sampling period is derived by dividing the frequency of the CBR stream 14A by n, using divider 34. Conveniently the counter reader 32 comprises a four bit gated latch. The value 36 read from the counter 24, which is in the range 0 to 15 (4 bits), forms one RTS value and is transmitted as part of the header of a number of ATM cells 6 to the destination exchange 10.

The frequency of the local oscillator 46 is set by calculating means 44 which calculates the source CBR frequency using the received RTS values and the network reference frequency 28. For a stable source CBR frequency the RTS value will change approximately linearly with time. The number of sampling periods required for the RTS value to change is related to the ratio of the network reference 28 and source CBR frequencies. Consequently the average rate of change of RTS value with time is related to the source frequency and can be used to calculate the source CBR frequency. Although, in theory, it is only necessary to count the number of received RTS values before the value changes in order to determine the rate of change of the RTS value, averaging over a large number of RTS values is actually required to achieve accurate frequency determination. The calculated frequency is used to maintain the frequency of the local oscillator 46. In this way the frequency of the local oscillator 46 is synchronised to the frequency of source CBR stream 2. Such a system however does not maintain the initial phase relation between the source 2 and recombined 12 CBR streams as adjustments are made to the local oscillator 46 frequency. Mathematical modelling for such a system in which the network reference frequency is 155.52MHz, the spot source CBR frequency is 2.048MHz, n=3008 and x=64 indicates that a phase error accumulation of approximately 5 bits can be expected during frequency synchronisation which occurs within approximately 0.3 seconds.

According to the present invention there is provided a synchronising circuit for use in a multiplexed packet based telecommunications network capable of carrying

Constant Bit Rate (CBR) data comprising: a local oscillator, a local Residual Time Stamp (RTS) generator arranged to determine a local RTS value from the local oscillator frequency, a comparator to determine the difference between the local RTS value and a source RTS value extracted from packets received at a destination exchange, and an oscillator controller responsive to the difference to adjust the frequency and phase of the local oscillator to maintain the difference constant.

Preferably the local RTS generator comprises a counter clocked by means of a clock derived from a network reference frequency, a $\div n$ divider to divide the frequency of the local oscillator by n , the output being connected to actuate a counter reader to read the counter output every n cycles of local oscillator frequency.

Advantageously the frequency of the local oscillator is adjusted by an amount (defined in bits s^{-1}) equal to the square of the difference and the phase of the local oscillator is adjusted by an amount (defined in bits) such that the phase stabilises at approximately the same time as frequency synchronisation.

According to another aspect of the present invention there is provided a method of synchronising the frequency, and maintaining the phase, of a CBR data stream formed at a destination exchange to that of a source CBR data stream, the method comprising: extracting a source Residual Time Stamp (RTS) from a received packet, generating a local RTS value from a local oscillator frequency, comparing the source and local RTS values and adjusting the frequency and phase of the local oscillator to maintain the difference constant.

Preferably the source and local RTS values are generated using the Synchronous Residual Time Stamp (SRTS) method.

Advantageously the frequency of the local oscillator is adjusted by an amount (defined in bits s^{-1}) equal to the square of the difference and the phase of the local oscillator is adjusted by an amount (defined in bits) such that the phase stabilises at approximately the same time as frequency synchronisation.

The invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 is a prior art Asynchronous Transfer Mode (ATM) packet based telecommunications network,

Figure 2 is a Residual Time Stamp (RTS) generator circuit which uses the Synchronous Residual Time Stamp (SRTS) method,

Figure 3 is a destination exchange including the synchronising circuit of the present invention and

Figure 4 shows the variation of local and source RTS values with time.

Referring to Figure 3 there is shown a destination

exchange 10 of an ATM packet based telecommunications network including a synchronising circuit for synchronising the frequency, and maintaining the phase relation, of a local oscillator 46 to that of the source CBR stream 2. ATM cells 6 arriving at the destination exchange 10 are buffered in a cell buffer 38. Information contained in the header of the ATM cell 6 is processed by cell header processor 40 to extract the source RTS value 41. This RTS value 41 is applied to a first input 52a of a comparator 52. A local RTS generator 50 calculates a local RTS value 51 using the frequency of the local oscillator 46 and the network reference frequency 23. The local RTS generator 50 uses the same method to generate the local RTS value 51 as that applied at the source exchange 4 to generate the source RTS value, for example the SRTS method as shown in Figure 2. The local RTS value 51 is compared with the source RTS value 41 by applying it to a second input 52b of the comparator 52. The output of the comparator 52 which represents the difference in RTS values is used by an oscillator controller 54 to adjust the frequency and phase of the local oscillator 46 to synchronise the frequency, and maintain the phase relation between the source CBR stream and local oscillator using a phased lock loop type method.

When the local oscillator 46 is in the same phase and at the same frequency as the source CBR stream 2, the local 51 and source 41 RTS values will be the same and will change with time in the same way. However in the majority of cases a phase difference will exist and it is desirable in an ATM network to maintain this difference rather than to minimise it. The phase difference is related to the difference between the RTS values, as shown in Figure 4. The phase relation between the source CBR stream 2 and the local oscillator 46 can therefore be maintained if this difference can be kept constant. This is achieved by oscillator controller 54 adjusting the phase 46a of the local oscillator 46 to maintain the difference between source 41 and local 51 RTS values.

The frequency of the source CBR stream 2 is related to the rate of change of source RTS with time, that is the gradient of the plot shown in Figure 4. Similarly the local oscillator frequency is related to the respective gradient of local RTS value versus time. To synchronise the frequency of the source CBR stream 2 and local oscillator 46 therefore requires these gradients to be the same. However rather than trying to maintain the gradients which requires averaging over a large number of values to determine frequency values, the oscillator controller 54 is arranged to adjust the frequency 46b of the local oscillator 46 to maintain the difference between the source 41 and local 51 RTS values. By maintaining the difference in RTS values the local RTS value will track the source RTS value and frequency synchronisation is achieved. Within Figure 4 frequency synchronisation is achieved at point A on the time axis.

Any algorithm can be applied by the oscillator controller 54 to determine how the local oscillator frequency

and phase should be adjusted according to the difference in RTS values. For example consider a network carrying CBR data streams with a spot frequency of 2.048 Mbits^{-1} and operating with a network reference frequency of $155.520 \text{ Mbits}^{-1}$. The value of x will be 64 ($155.52 \div 2.048 = 75.94 = 2^6$) and $n = 3008$ ($47 \times 8 \times 8 =$ No of octets \times No of bits \times No of cells between determining RTS value). In such a network the oscillator controller 54 is arranged to adjust the phase of the local oscillator 46 by one fifteenth of a bit and adjust the frequency by an amount (defined in bits s^{-1}) equal to the square of the difference between the two RTS values. With this algorithm frequency synchronisation and phase stabilisation from the worst case situation (that is 50ppm of the spot frequency - 2.0479 Mhz) is achieved within 0.3 seconds with a residual phase error of less than 0.3 bits. The phase increment of one fifteenth of a bit is selected to ensure that the phase relation also stabilises at approximately the same time as frequency synchronisation, that is within 0.3 seconds.

It is preferred to apply the algorithm in an initial period to every received RTS value for rapid synchronisation and then only make adjustments periodically after a predetermined number of cells to reduce jitter accumulation. To reduce the effect that a corrupt source RTS value could have on the operation of the system the cell header processor checks the received RTS value to validate it. When a corrupt RTS value is detected a control signal 56 is passed to the oscillator controller 54. The oscillator controller 54 is configured upon receipt of such a signal 56 to either disable operation and maintain the current local oscillator frequency and phase, or to predict a value for the source RTS based on the history of previously received values and adjust the frequency and phase of the local oscillator based on this value. The cell header processor 40 can validate an RTS value since limits can be predicted as to how rapidly the RTS value will change with time. If a change in received RTS value is outside these limits the RTS value is assumed to have been corrupted. In the present example this ensures that (at least) one corrupt value can be detected and ignored, although this is at the expense of precision in the resolution of the source frequency.

An advantage of the present invention is that both the local and source RTS values are subject to the same effects of noise and therefore these effects tend to cancel out. This noise effect is caused when rounding or quantising the RTS value to the nearest integer.

Claims

1. A synchronising circuit for use in a multiplexed packet based telecommunications network capable of carrying Constant Bit Rate (CBR) data comprising: a local oscillator (46), a local Residual Time Stamp (RTS) generator (50) arranged to determine a local RTS value (51) from the local oscillator frequency, a comparator (52) to determine the difference between the local RTS value (51) and a source RTS value (41) extracted from packets received at a destination exchange (10), and an oscillator controller (54) responsive to the difference to adjust the frequency and phase of the local oscillator to maintain the difference constant.
2. A synchronising circuit according to claim 1 in which the local RTS generator (50) comprises a counter (32) clocked by means of a clock (26) derived from a network reference frequency (28), a $\div n$ divider (34) to divide the frequency of the local oscillator (46) by n , the output being connected to actuate a counter reader (32) to read the counter output every n cycles of local oscillator frequency.
3. A synchronising circuit according to any preceding claim in which the frequency of the local oscillator is adjusted by an amount (defined in bits s^{-1}) equal to the square of the difference.
4. A synchronising circuit according to any preceding claim in which the phase of the local oscillator is adjusted by an amount (defined in bits) such that the phase stabilises at approximately the same time as frequency synchronisation.
5. A method of synchronising the frequency, and maintaining the phase, of a CBR data stream (12) formed at a destination exchange (10) to that of a source CBR data stream (2), the method comprising: extracting a source Residual Time Stamp (RTS) (41) from a received packet (6), generating a local RTS value (51) from a local oscillator frequency, comparing the source and local RTS values and adjusting the frequency and phase of the local oscillator to maintain the difference constant.
6. A method according to claim 5 in which the source and local RTS values are generated using the Synchronous Residual Time Stamp (SRTS) method.
7. A method according to claims 5 or 6 in which the frequency of the local oscillator is adjusted by an amount (defined in bits s^{-1}) equal to the square of the difference.
8. A method according to claims 5, 6 or 7 in which the phase of the local oscillator is adjusted by an amount (defined in bits) such that the phase stabilises at approximately the same time as frequency synchronisation.
1. A synchronising circuit for use in a multiplexed packet based telecommunications network capable of carrying Constant Bit Rate (CBR) data comprising: a local oscillator (46), a local Residual Time Stamp (RTS) generator (50) arranged to determine a local RTS value (51) from the local oscillator frequency,

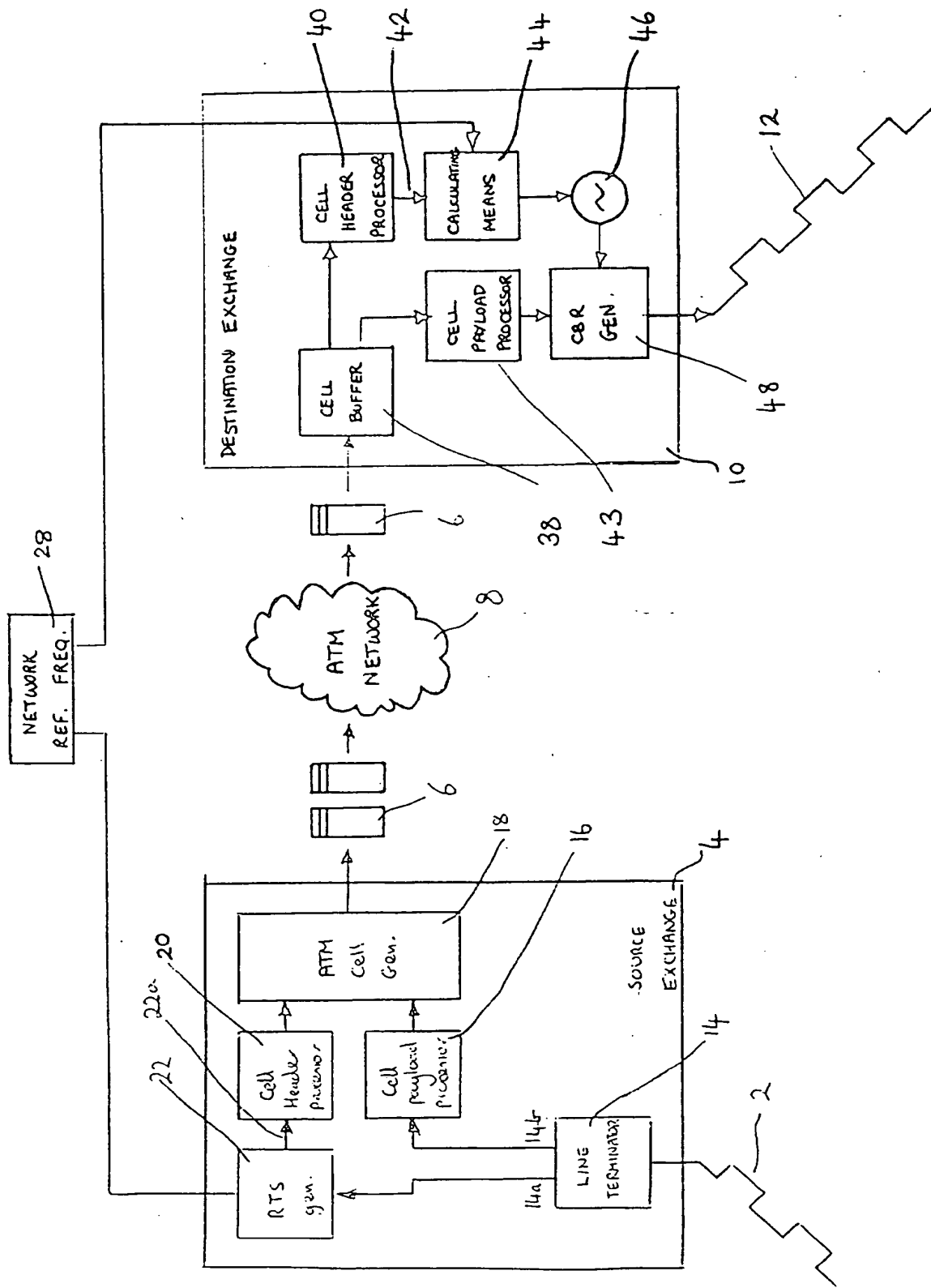


Figure 1

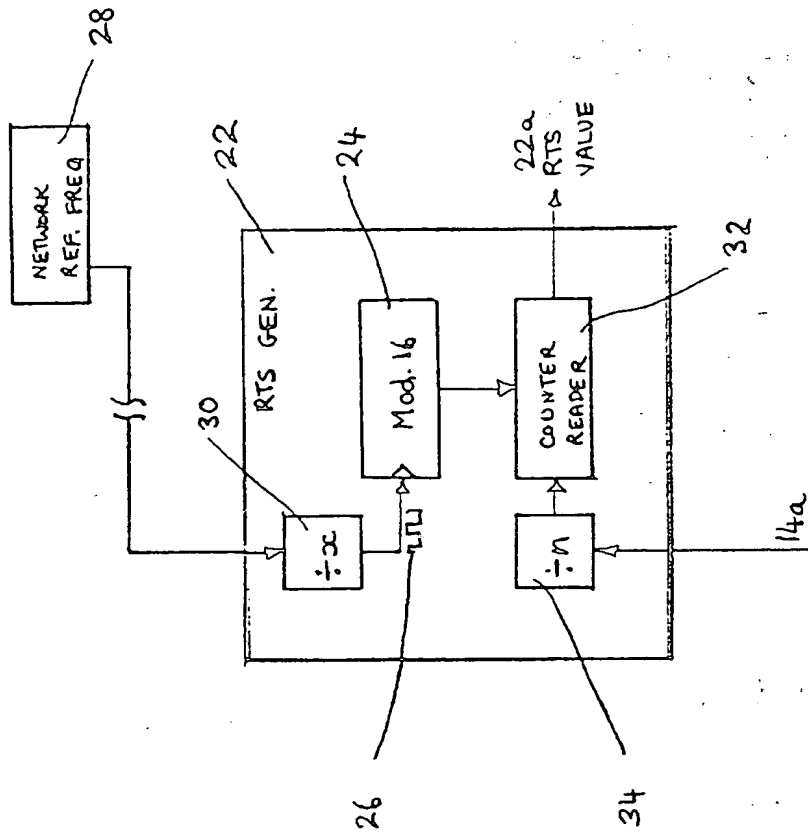


Figure 2

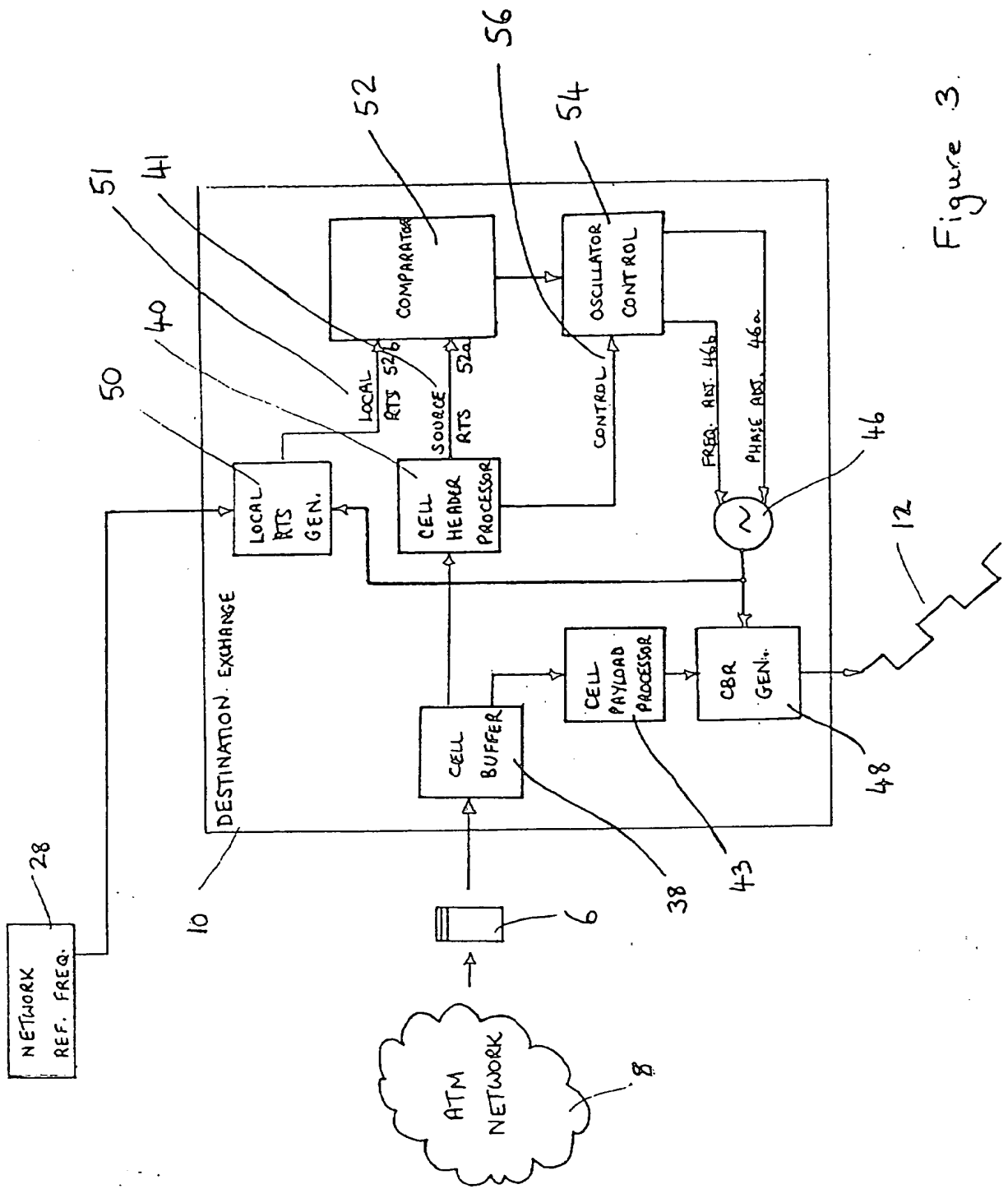


Figure 3.

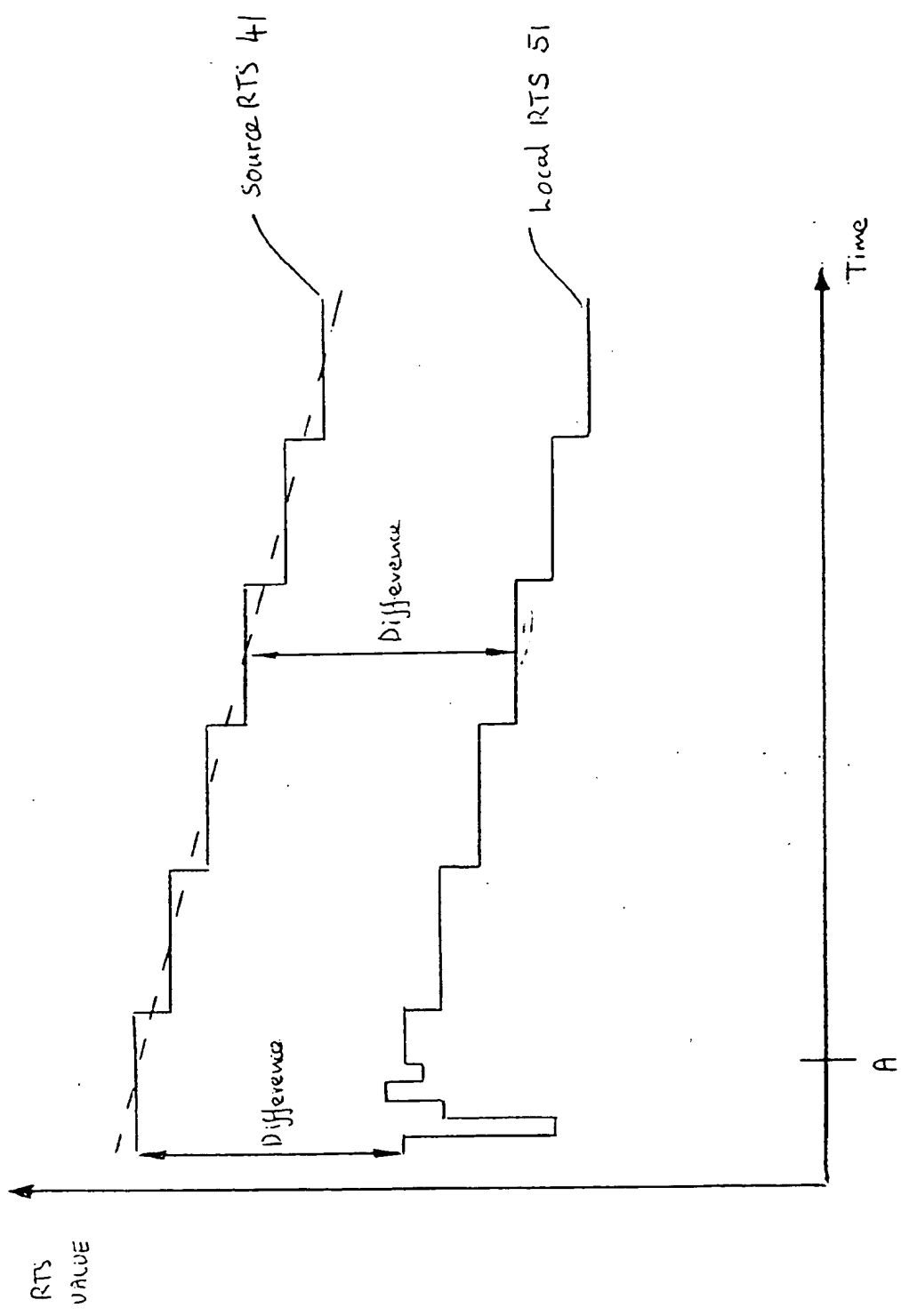


Figure 4